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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,222	08/01/2001	Robert B. Davies	4151-A4	5846

7590 04/07/2004

Robert A. Parsons
PARSONS & GOLTRY
Suite 260
340 East Palm Lane
Phoenix, AZ 85004

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,222	DAVIES, ROBERT B.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,28-33 and 37-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,28-33 and 37-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/1/01* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 12/22/03, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the sealed cavity ... and in communication with a lower portion of the high conductivity material in the trench (claims 43 and 45) must be shown or the feature(s) canceled from the claim(s). It is further unclear what the limitation "in communication" is referring to, whether the lower portion is contacting the sealed cavity or that the sealed cavity and lower portion are on the same substrate. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 47 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 47 recites the limitation "the pedestal" in line 3 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 thru 3, 5 thru 7, 37 thru 40, 42, 43, 45, and 47 thru 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall 3,881,244 in view of Riseman 4,169,000. Kendall discloses (see, for example, FIG. 15) an integrated circuit comprising a silicon substrate (low resistivity semiconductor substrate) 2, dielectric region, trench, oxide layer (dielectric sidewalls) 7, isolation region 25', and core material (conductive material) 12. The right side of the figure clearly shows an inductance I. Kendall does not disclose the isolation region 25' as a cavity. However, Riseman discloses (FIG. 7) an integrated circuit structure comprising a cavity 12. In column 4, lines 32-37, Riseman

discloses the cavity as being air isolated and capable of absorbing changes in volume resulting from processing steps. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the cavity of Riseman in Kendall's invention in order to absorb changes in volume resulting from processing steps.

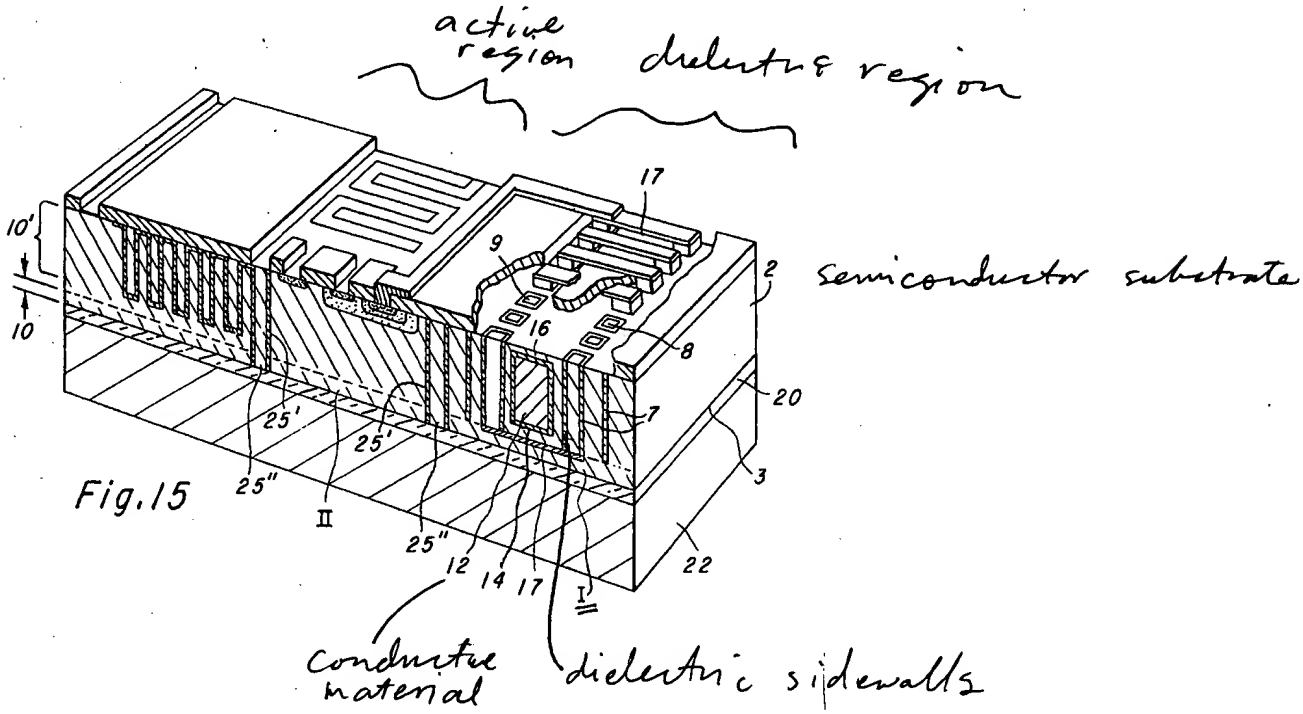

Fig. 15

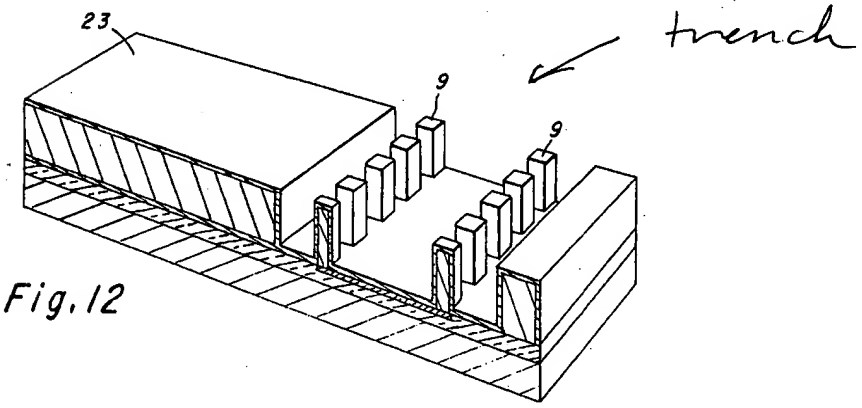

Fig. 12

Regarding claim 5, see column 3, lines 23-25 wherein the grooves are stated as 15 mils (37.5 microns) deep.

Regarding claims 37, 38, 42, 43, 45 and 49, Kendall discloses (see, for example, FIG. 15) an integrated circuit comprising a silicon substrate (low resistivity semiconductor substrate) 2, transistor element (active region) II, dielectric region, transistor (active component), trench, oxide layer (side-walls) 7, and metal core (high conductivity electroplated material) 12. The dielectric region is the general area where isolation layer 14 is present (the area where the transistor is not). Multiple cavities are formed that include oxide layer 7 and layers 25'.

Regarding claims 39, 40, 47, 48, and 50, Kendall does not disclose the dielectric material and the array of cavities produce an effective dielectric constant at least ten percent lower than the first dielectric constant and wherein the effective dielectric constant is approximately 2.5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use these value, since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

7. Claims 4, 41 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall '244 in view of Riseman '000 as applied to claims 1-3, 5-7, 37-40, 42, 43, 45, and 47-50 above, and further in view of Matsuzaki 06-120036. Kendall in view of Riseman does not disclose the conductive material including copper. However, Matsuzaki discloses a semiconductor device comprising a trench 31 filled with copper. The copper serves as a conductive metal for an induction element such as an inductor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use copper in order to form an inductor with good inductive properties and increased current capacity.

8. Claims 28 thru 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki 06-120036 JPO in view of Kendall 3,881,244 in view Riseman 4,169,000. Matsuzaki discloses (see, for example, figure 2) a semiconductor device comprising a substrate 61, insulating film (dielectric region) 32, and trench 31 filled with a high conductive material (first inductor and second inductor of electroplated conductive material). A first inductor is formed in the substrate 61 and a second inductor is formed in substrate 11. Matsuzaki does not disclose a cavity. However, Kendall discloses (see, for example, FIG. 15) a semiconductor device comprising an inductor I and an isolation region (cavity) 25. Kendall teaches (see, for example, column 7, lines 22-49) that this isolation region isolates different parts in an integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the isolation region (cavity) in order to isolate different parts of an integrated circuit so that no interference occurs between adjacent devices.

Matsuzaki in view of Kendall does not disclose the isolation region 25 as a cavity. However, Riseman discloses (FIG. 7) an integrated circuit structure comprising a cavity 12. In column 4, lines 32-37, Riseman discloses the cavity as being air isolated and capable of absorbing changes in volume resulting from processing steps. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the cavity of Riseman in order to absorb changes in volume resulting from processing steps.

Regarding claims 31 and 32, see page 5 of translation wherein Matsuzaki discloses the coil as hundreds of micrometers.

9. Claims 44 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall 3,881,244 in view of Riseman '000 as applied to claims 1-3, 5-7, 37-40, 42, 43, 45, and 47 thru 50 above, and further in view of Farooq et al. 6,574,859 B2. Kendall in view of Riseman does not disclose a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity. However, Farooq discloses (see, for example, FIG. 1A) a circuit card (die attach pad) 10 connected to a substrate 4. The circuit card makes a card assembly so that a more complicated integrated circuitry is formed. It would have been obvious to one of ordinary skill in the art at the time of invention to include the circuit card (die attach pad) in order to form a more complicated integrated circuitry such as an IC card.

Product-by-Process Limitations

10. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Response to Arguments

11. Applicant's arguments with respect to claims 1-7, 28-33, and 37-51 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant's argument on page 8, lines 1-4 that Kendall discloses a solid state conductor and not an integrated circuit, this argument is not persuasive. In column 1, lines 27-35, Kendall clearly states the object of the invention is to provide an integrated circuit having a semiconductor inductor therein. Because it does not state

"integrated circuit" in the title does not mean Kendall does not disclose an integrated circuit.

Regarding applicant's argument on page 9, last paragraph that no reasonable interpretation of the term "inductance" would allow the Examiner to say that " an inductance is formed in the core" of an electrical coil, this argument is not persuasive. In column 8, lines 66-67, Kendall disclose the core material 12 being chosen with a high permeability to provide a relatively high inductance. Clearly, the core material of Kendall has an inductance.

Regarding applicant's argument on page 10, second paragraph that Kendall does not show a trench having dielectric sidewalls and the inductance bounded by the sidewalls, this argument is not persuasive. In Fig. 15, Kendall discloses an inductor core 12 that is bounded by the oxide layer (dielectric sidewalls) 7. The trench is more clearly shown in Fig. 12 wherein a trench is formed between the studs 9. The trench is then coated on its sidewalls by the oxide layer 7. See the 102 rejection (see the labeled figures in paragraph 6) above.

Regarding applicant's argument on page 11, second paragraph that Kendall's inductance includes studs 9 and metal interconnects 17, none of which are bounded by a trench sidewall, this argument is not persuasive. The applicant's claims only state an INDUCTANCE which is a property, not an entire inductor device, therefore, since core 12 clearly has at least an inductance, Kendall discloses an inductance bounded by dielectric sidewalls.

Regarding the applicant's argument on page 14, last paragraph that electroplated conductive material is a specific type of material and that many conductive materials

cannot be electroplated, this argument is not persuasive. The Examiner agrees that many different materials can not be electroplated, however, in this case, Kendall discloses (see, for example, column 4, line 28) the core (conductive material) 12 as being metallic. Metallic materials clearly can be electroplated.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

Eugene Lee
March 31, 2004